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Notice of Allowability	Application No.	Applicant(s)
	10/707,564 Examiner	HSU ET AL. Art Unit
	Lammer	Art Offic
	David Lam	2827
The MAILING DATE of this communication appeal All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIOF the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this apport or other appropriate communication IGHTS. This application is subject to	plication. If not included will be mailed in due course. THIS
1. This communication is responsive to		
2. The allowed claim(s) is/are <u>1-20</u> .		
3. The drawings filed on 22 December 2003 are accepted by	the Examiner.	
 4. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)		
 Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO-1449 or PTO/SB/O Paper No./Mail Date	6. Interview Summary Paper No./Mail Da 08), 7. Examiner's Amendo	te
		DAVID LAM PRIMARY EXAMINER

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Allowable Subject Matter

1. The following is an examiner's statement of reasons for allowance: Claims 1-20 are allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach: method for writing a memory module comprising step of applying a bit line voltage to the bit line of the memory cell to be written so that a hot hole in the p-type channel of the memory cell to be written includes hot electrons to be injected into stacked dielectric layer of the memory cell to be written, and among other steps as claimed in independent claim 1.

Method of reading comprising step of applying a bit line voltage to the bit line connected to the memory cell to be read in order to enlarge a depletion region between the p-type drain or the p-type source and the substrate of the memory cell to be read, and among other steps as claimed in independent claim 8. Method of erasing comprising step of applying a voltage equivalent to the source line voltage to the substrates of the plurality of memory cells, and among other steps as claimed in independent claim 15.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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- Hirano (6,657,898) discloses a nonvolatile semiconductor memory device and data

erase method therefor.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to David Lam whose telephone number is 571-272-1782. The

examiner can normally be reached on 6:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone numbers for the

organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Lam

DAVID LAW

April 15, 2005